DRAM MEMORY INTEGRATION METHOD

Abstract of the Disclosure

The invention relates to a DRAM integration method that does away with the alignment margins inherent to the photoetching step of the upper electrode of the capacitance for inserting the bit line contact. The removal of the upper electrode is self-aligned on the lower electrode of the capacitance. This is accomplished by forming a difference in topography at the point where the opening of the upper electrode is to be made, and depositing a non-doped polysilicon layer on the upper electrode. An implantation of dopants is performed on this layer, and the part of the non-doped layer located in the lower part of the zone showing the difference in topography is selectively etched. The remainder of the polysilicon layer and the part of the upper electrode located in the lower layer are also etched.